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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,958	03/10/2000	Katsuhiko Asai	15162/01590	4595

24367 7590 06/25/2002

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EXAMINER
MAIER, CHRISTOPHER J

ART UNIT	PAPER NUMBER
2675	9

DATE MAILED: 06/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/522,958	Applicant(s) ASAI ET AL.	
	Examiner Christopher J. Maier	Art Unit 2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4 and 7* is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-18,23,24,26 and 28-30* is/are rejected.

7)☒ Claim(s) *19-22 25 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-11,13,16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (U.S. Patent No. 5,515,080) in view of Yuan et al (6,317,189 B1).

As to claim 1, Nakamura discloses a driving circuit which performs writing on the liquid crystal display in column 4, lines 35-44. Nakamura also discloses a data processing unit which is connected to the driving circuit in column 1, lines 56-60. Nakamura discloses a power supply circuit which supplies electric power to the driving circuit and the data processing unit in figure 1, item 30 and column 4, lines 36-54. Nakamura also discloses a controller which inactivates at least part of the power supply circuit and/or at least part of an internal circuit of the data processing unit after writing on the liquid crystal display in figure 3 and column 5, lines 66-67 and column 6, lies 1-37.

Nakamura does not disclose a liquid crystal display (LCD) with a reflective type liquid crystal with a memory effect.

Yuan discloses an LCD with a reflective type liquid crystal with a memory effect in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 2, Nakamura discloses that the power supply circuit includes a booster circuit in figure 3, items 93 and 95 and column 6, lines 13-18. Nakamura further discloses that the controller inactivates the booster circuit after writing on the LCD in column 6, lines 1-37.

As to claim 5, Nakamura discloses that the power conservation method does not include a power switch for turning on and off a main power source in figure 3, item 83 and column 6, lines 1-6. Nakamura uses a sleep circuit, as depicted in figure, which is independent of the main power source switch illustrated in figure 1, item 30 and column 4, lines 35-59. The sleep circuit is housed in the display controller (item 24 of figure 1) and is inputted a signal from timer 81 of figure 2.

As to claim 6, Nakamura does not disclose an LCD which exhibits a cholesteric phase.

Yuan discloses an LCD which exhibits a cholesteric phase in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 8, Nakamura does not disclose that unchangeable information is displayed on the LCD.

Yuan discloses that unchangeable information is displayed on the LCD in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the cholesteric, reflective display with of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 9, Nakamura discloses an operation section with which a user is capable of making an input and wherein writing on the liquid crystal display is carried out in accordance with the input made with the operation section in column 2, lines 45-55 and column 8, lines 40-67.

As to claim 10, Nakamura discloses that inactivation of at least part of the internal circuit of the data processing unit is inhibited while an input is being continuously made with the operation section in column 2, lines 45-55 and column 8, lines 40-67.

As to claim 11, Nakamura discloses a receiving circuit which receives a signal from outside, wherein information about reception of a signal at the receiving circuit is displayed on the liquid crystal display in column 2, lines 45-55 and column 8, lines 40-67.

As to claim 13, Nakamura discloses that the controller inactivates at least part of the power supply circuit a specified time after writing on the LCD in column 8, lines 40-67.

As to claim 16, Nakamura discloses that after writing on the LCD, inactivating at least part of a power supply circuit which supplies electric power to a driving circuit which performs writing on the LCD and/or at least part of an internal circuit of a data processing unit which is connected to the driving circuit in column 8, lines 40-67.

Nakamura does not disclose that the LCD uses a reflective type liquid crystal with a memory effect.

Yuan discloses an LCD with a reflective type liquid crystal with a memory effect in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Hawkins with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 18, Nakamura discloses that the controller inactivates at least part of the power supply circuit a specified time after writing on the LCD in column 8, lines 40-67.

As to claim 28, Nakamura discloses a driving circuit which performs writing on the liquid crystal display in column 4, lines 35-44. Nakamura also discloses a data processing unit which is connected to the driving circuit in column 1, lines 56-60. Nakamura discloses a power supply circuit which supplies electric power to the driving circuit and the data processing unit in figure 1, item 30 and column 4, lines 36-54. Nakamura also discloses a controller which inactivates at least part of the power supply circuit and/or at least part of an internal circuit of the data processing unit after writing

on the liquid crystal display in figure 3 and column 5, lines 66-67 and column 6, lies 1-37.

Nakamura does not disclose a liquid crystal display (LCD) with a reflective type liquid crystal with a memory effect.

Yuan discloses an LCD with a reflective type liquid crystal with a memory effect in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 29, Nakamura discloses that power supply from the power supply circuit to the driving circuit is inhibited by the controller in figure 3 and column 5, lines 66-67 and column 6, lies 1-37.

As to claim 30, Nakamura does not disclose an LCD which exhibits a cholesteric phase.

Yuan discloses an LCD which exhibits a cholesteric phase in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

2. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Yuan, and in further view of Hawkins (U.S. Patent No. 5,133,076).

As to claim 15, Nakamura discloses a driving circuit which performs writing on the liquid crystal display in column 4, lines 35-44. Nakamura also discloses a data processing unit which is connected to the driving circuit in column 1, lines 56-60. Nakamura discloses a power supply circuit which supplies electric power to the driving circuit and the data processing unit in figure 1, item 30 and column 4, lines 36-54. Nakamura also discloses a controller which inactivates at least part of the power supply circuit and/or at least part of an internal circuit of the data processing unit after writing on the liquid crystal display in figure 3 and column 5, lines 66-67 and column 6, lies 1-37.

Nakamura does not disclose an LCD with a reflective type liquid crystal with a memory effect or a casing which encases the LCD, the driving circuit, the data processing unit, the power supply circuit and the controller.

Yuan discloses an LCD with a reflective type liquid crystal with a memory effect in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

Hawkins discloses an LCD with a casing which encases the LCD, the driving circuit, the data processing unit, the power supply circuit and the controller in figure 1 and figure 5, as well as in column 1, lines 61-65.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan and the encased display of Hawkins with the power saving method of Nakamura because reflective type displays are common in the art and additionally Hawkins has a power conservation mode in column 8, lines 42-58. Also, Yuan discloses that his display is portable in column 1,

lines 19-21, and consequently, it would need to have some sort of casing. Additionally, it would have been obvious to include the casing for the LCD device of Nakamura, as in Hawkins, in order to protect the interior of the device.

As to claim 23, Nakamura does not disclose an LCD which exhibits a cholesteric phase.

Yuan discloses an LCD which exhibits a cholesteric phase in figure 7, item 80, column 11, lines 39-46 and column 13, lines 26-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 24, Nakamura dose not disclose that the LCD includes a pair of substrates accommodating the reflective type LCD therebetween.

Yuan discloses a pair of substrates accommodating the reflective type LCD in figures 3a-3f, item 42, and column 6, lines 33-37.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

As to claim 26, Nakamura does not disclose that a plurality of resin pillars are provided between the substrates.

Yuan discloses a plurality of resin pillars provided between the substratesin column 7, lines 20-25.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the reflective display of Yuan with the power saving method of Nakamura because reflective type displays are common in the art.

3. Claims 12, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Yuan in view of Ho (U.S. Patent No. 5,757,365).

As to claims 12 and 17, as dependent on claims 1 and 16, respectively, neither Nakamura nor Yuan discloses that the controller inactivates at least part of the power supply circuit immediately after writing on the LCD.

Ho discloses that the controller inactivates at least part of the power supply circuit immediately after writing on the LCD in column 1, lines 42-54.

It would have been obvious to one having ordinary skill in art at the time of invention to combine the display methods of Nakamura and Yuan with the display inactivation method of Ho in order to conserve more power when the displaying of new information is not occurring.

As to claim 14, Nakamura discloses the controller inactivates at least part of the power supply circuit a specified time after writing on the LCD in column 8, lines 40-67.

Neither Nakamura nor Yuan disclose that the controller inactivates at least part of the power supply circuit immediately after writing on the LCD.

Ho discloses that the controller inactivates at least part of the power supply circuit immediately after writing on the LCD in column 1, lines 42-54.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the delayed circuit inactivation of Nakamura with the immediate circuit inactivation of Ho in order to have a write mode wherein the display is conserving power following each write period and a write mode wherein write speed is increased by conserving less power.

Response to Amendment

4. With respect to Applicant's argument regarding claims 1, 2, 5, 6, 8-11 and 13 that Nakamura does not disclose or suggest a "controller which inactivates at least part of the power supply circuit after writing on the liquid crystal display," I respectfully disagree. Nakamura states in column 3, lines 1-4, that "power consumption required for reading out display data from the VRAM, and writing data on a display device can be saved while the TFT LCD maintains its display content." Further, in column 6, lines 29-37, Nakamura discloses that counters 85, 87, 89 and 91 of figure 3 are sent a sleep signal, wherein the counters do not use any power. As such, part of the power supply circuit is deactivated while these are in sleep state.

5. With respect to Applicant's argument regarding claims 3, 4 and 7, Nakamura does not disclose that either of the central processing units are inactivated during any stage of processing, as such, these claims are allowable over the prior art.

6. With respect to Applicant's argument regarding claims 16 and 18, please see the response to claims 1, 2, 5, 6, 8-11 and 13 above.

7. With respect to Applicant's argument regarding claim 15, please see the response to claims 1, 2, 5, 6, 8-11 and 13 above.

8. With respect to Applicant's argument regarding claims 12, 14 and 17, please see the response to claims 1, 2, 5, 6, 8-11 and 13 above.

Allowable Subject Matter

9. Claims 3,4 and 7 are allowed.

10. Claims 19-22, 25 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris Maier, whose telephone number is (703) 605-1213 and whose normal working hours are 7:30AM – 4PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

cjm
June 21, 2002

Chris Maier

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600